**What is claimed is:**

1. A method of fabricating a nitride read only memory, comprising the steps of:

providing a semiconductor substrate, comprising a memory region and a peripheral circuit region therein;

growing a pad oxide on the semiconductor substrate;

forming a plurality of parallel buried diffusion regions as bit lines in the memory region;

forming a first shallow trench and a second shallow trench in the peripheral circuit region;

conformally forming an ONO film on the semiconductor substrate;

depositing a polysilicon layer on the ONO film to fill the first shallow trenches and the second shallow trench;

selectively etching the polysilicon layer in the memory region to define a plurality of polysilicon structures as word lines having gaps therein, and removing the polysilicon from the first shallow trenches and leaving the polysilicon layer in the second shallow trench in the peripheral circuit region; and

forming an insulator in the first shallow trenches and the gaps between the word lines.

2. The method as claimed in claim 1, further comprising:

planarizing the insulator to leave shallow trench isolations in the first shallow trenches and between the word lines;

selectively etching the polysilicon structures and the ONO layer to expose the semiconductor substrate between the first shallow trenches; and

implanting dopants into the substrate between the first shallow trenches to define the well regions.

3. The method as claimed in claim 1, wherein the bit lines formation further comprises:

forming a first photoresist pattern with a plurality of parallel first openings on the pad oxide in the memory region to serve as bit line mask;

implanting dopants into the semiconductor substrate to form a plurality of parallel buried diffusion regions as bit lines in the memory region; and

removing the bit line mask.

4. The method as claimed in claim 1, wherein the first and the second shallow trench formation further comprises:

forming a second photoresist pattern on the pad oxide, wherein the second photoresist pattern has second openings in the peripheral circuit region;

selectively etching the semiconductor substrate through the second openings to create a first shallow trenche and a second shallow trench; and

removing the second photoresist pattern and the pad oxide.

5. The method as claimed in claim 1, wherein the semiconductor substrate is a silicon substrate.

6. The method as claimed in claim 1, wherein the semiconductor substrate is a silicon-on-insulator (SOI) substrate.

7. The method as claimed in claim 1, wherein the pad oxide is formed by thermal oxidation.

8. The method as claimed in claim 1, wherein the buried diffusion regions are formed by implanting n-type ions in the semiconductor substrate.

9. The method as claimed in claim 1, wherein the buried diffusion region is implanted before the ONO layer is formed.

10. The method as claimed in claim 1, wherein the buried diffusion region is implanted after the ONO layer is formed.

11. The method as claimed in claim 1, further comprising rapid thermal anneraling (RTA) after implantation to activate the dopants in the substrate.

12. The method as claimed in claim 1, wherein the bit line mask is a patterned photoresist.

13. The method as claimed in claim 1, wherein thickness of the ONO layer is between about 150 and 250Å.

14. The method as claimed in claim 1, wherein the ONO layer is further formed on the sidewall of the shallow trench to avoid STI corner recess.

15. The method as claimed in claim 1, wherein the ONO layer is further formed on the sidewall of the shallow trench to avoid deformation of the STI profile during thermal process.

16. The method as claimed in claim 1, wherein the insulator is a silicon dioxide layer.

17. The apparatus as claimed in claim 16, wherein the polysilicon layer comprises a dopant polysilicon layer.

18. The method as claimed in claim 1, wherein the insulator is formed by high density plasma chemical vapor deposition (HDPCVD).

19. The method as claimed in claim 2, wherein the insulator is planarized by chemical mechanical polishing.